Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.071”**

**PAD FUNCTIONS:**

1. **COMP**
2. **VFB**
3. **ISENSE**
4. **RT/CT**
5. **PWR GND**
6. **GND**
7. **OUTPUT**
8. **VC**
9. **VCC**
10. **VREF**

**1845A**

**.101”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: GND**

**Mask Ref: 1845A**

**APPROVED BY: KW DIE SIZE .071 X .101” DATE: 1/24/23**

**MFG: TEXAS INSTRUMENTS THICKNESS: .015” P/N: UC3845A**

**DG 10.1.2**

#### Rev B, 7/19/02